REMARKS

The present Amendment cancels claims 1-13 and adds new claims 14-21. Therefore, the present application has pending claims 14-21.

Claims 12 and 13 stand rejected under 35 USC §102(e) as being anticipated by Barrientos (U.S. Patent No. 5,910,899) and claims 1-11 stand rejected under 35 USC §103(a) as being unpatentable over Barrientos in view of Ramachandran (U.S. Patent No. 6,002,857). As indicated above, claims 1-13 were canceled. Therefore, these rejections are rendered moot. Accordingly, reconsideration and withdrawal of these rejections is respectfully requested.

As indicated above, claims 1-13 were canceled and new claims 14-21 were added. New claims 14-21 are directed to several embodiments of an information processing system.

The first embodiment of the present invention provides an information processing system having a first input unit for receiving, from external of the information processing unit, circuit information of a module having a semiconductor integrated circuit, a floorplan which is allocation information of blocks constituting the module and evaluation and indices for evaluating modifications of the floorplan, wherein the circuit information, the floorplan information and the evaluation indices are associated with each other, a storing unit for storing the associated circuit information, floorplan information and evaluation indices, a second input unit for inputting specifications for modifying the floor plan and a processing unit for modifying the floorplan according to the specifications to evaluate the modified floorplan according to the evaluation indices.

The second embodiment is similar to the first embodiment but provides that the processing unit reads the floorplan stored in the storing unit according to specification information when the specification information for modifying the floorplan is input,

generating a plurality of floorplan candidate each being modified based on the read floorplan and the specification information, evaluating the generated floorplan candidates based on the evaluation indices and selecting one floorplan based on the evaluation result.

A third embodiment provides an information processing system for designing a semiconductor integrated circuit having a storing unit for storing circuit information of a module constituting the semiconductor integrated unit, a floorplan which is allocation information of blocks constituting the module and evaluation indices for evaluating modifications of the floorplan wherein the circuit information, the floorplan and the evaluation indices are associated with each other and input/output unit for transmitting the associated circuit information floorplan and evaluation indices from the storage unit.

A fourth embodiment of the present invention provides an information processing system used for designing a semiconductor integrated circuit having a circuit designing apparatus and a floorplan modifying apparatus.

The circuit designing apparatus includes a first storing unit for storing circuit information of a module constituting the semiconductor integrated circuit, a floorplan which is allocation information of blocks constituting the module and evaluation indices for evaluating modifications of the floorplan wherein the circuit information, floorplan and evaluation indices are associated with each other and a first input/output unit for transmitting the stored circuit information, floorplan and evaluation indices.

The floorplan modifying apparatus includes an input unit for inputting information for modifying the floorplan, a second input/output unit for receiving the circuit information floorplan and evaluation indices transmitted from the circuit designing apparatus, a second storing unit for storing the circuit information, and evaluation indices received by the second input/output unit and a processing unit for modifying the floorplan according

to the information input by the input unit and for evaluating the modified floorplan based on the evaluation indices.

The above described features of the present invention now more clearly recited in new claims 14-21 are not taught or suggested by any of the references of record whether taken individually or in combination with each other. Particularly, the above described features of the present invention now recited in new claims 14-21 are not taught or suggested by Barrientos or Ramachandran whether taken individually or in combination with each other as suggested by the Examiner.

As is clear from above, the unique features of the present invention is that circuit information of a module constituting a semiconductor integrated circuit, a floorplan and a evaluation indices are input to the information processing system from external of the information processing system. Further, the circuit information, floorplan and evaluation indices are associated with each other.

Thus, by use of the features of the present invention as described above it is possible to automatically use the floorplan and evaluation indices which are appropriate to the circuit information since such information have been previously associated with each other. According to the present invention a user having no knowledge of design techniques for designing a semiconductor integrated circuit can easily modify the floorplan of the semiconductor integrated circuit by viewing the circuit information, floorplan and evaluation indices since such have been previously associated with each other. Therefore, by use of the present invention there is no reduction in the ability to design efficient and effective semiconductor integrated circuits whether the expert designer is designing such circuit or a novice.

The above described features of the present invention are not taught or suggested by the references of record particularly Barrientos and Ramachandran.

Therefore, the features of the present invention as now recited in the claims are not anticipated by any one of Barrientos and Ramachandran or rendered obvious by the combination of Barrientos or Ramachandran or any of the other references of record.

Barrientos discloses a computer implemented method for aiding in the design of an integrated circuit floorplan. Barrientos makes use of circuit information, floorplan and evaluation indices similar to that of the present invention. However, the similarity ends there. According to the present invention, the circuit information, floorplan and evaluation indices are input from external of the information processing system and the circuit information, floorplan and evaluation indices are previously associated with each other. Such features are clearly not taught or suggested by Barrientos.

Thus, Barrientos suffers from the problems of the conventional apparatus to which the present invention was intended to solve. Namely, to allow users who are not experienced in integrated circuit design to be able to easily modify and design a semiconductor integrated circuit. The present invention accomplishes such by allowing the circuit information, floorplan and evaluation indices to be input from external of the system and to have the circuit information, floorplan and evaluation indices be previously related to each other. Such features are clearly not taught or suggested by Barrientos.

The above noted deficiencies of Barrientos are not supplied by Ramachandran. Therefore, the combination of Barrientos and Ramachandran still fails to teach or suggest the features of the present invention as recited in the claims.

Ramachandran merely discloses a method and apparatus of generating a plurality of floorplans and selecting one of the floorplans based on evaluation indices. However, similar to Barrientos, Ramachandran fails to teach or suggest the inputting from external of the system circuit information, floorplan and evaluation indices and the

predetermined association of the circuit information, floorplan and evaluation indices to each other as in the present invention.

Therefore, Ramachandran suffers from the same deficiencies relative to the present invention as Barrientos. Accordingly, the combination of Barrientos and Ramachandran does not render obvious the features of the invention as new recited in claims 14-21.

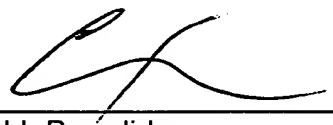
The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 1-13.

In view of the foregoing amendments and remarks, Applicants submit that claims 14-21 are in condition for allowance. Accordingly, early allowance of claims 14-21 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.38174X00).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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